CLAIMS

We claim:

1.   A clock network for an integrated circuit comprising:

a first set of lines configured to distributes clock signals to a first section of the integrated circuit;

a second set of lines configured to distribute clock signals to a second section of the integrated circuit separately from the first section of the integrated circuit; and

a third set of lines configured to distribute clock signals to both the first and second sections of the integrated circuit.

2.   The clock network of claim 1 further comprising:

at least one line disposed in the first section that connects to the first and third sets of lines; and

at least one line disposed in the second section that connects to the second and third sets of lines.

3.   The clock network of claim 2, wherein the first and third sets of lines converge at the center of the first section, and wherein the second and third sets of lines converge at the center of the second section.

4.   The clock network of claim 2, wherein the at least one line disposed in the first section is connected directly to an input/output (I/O) of the integrated circuit to receive an input-clock signal.

5.   The clock network of claim 3, wherein the integrated circuit includes a plurality of logic resources, wherein the at least one line in the first section connects to the plurality of logic resources in the first section , and wherein the at least one line in the second section connects to the plurality of logic resources in the second section.

6.   The clock network of claim 1, wherein the integrated circuit includes a plurality of logic resources, and wherein the third set of lines is configured to receive an input-clock signal from at least one logic resource.

7.   The clock network of claim 6, wherein the third set of lines is connected to a sneak path from the at least one logic resource.

8.   The clock network of claim 6, wherein the third set of lines is configured to receive an input-clock signal from a dedicated input-clock pin.

9.   The clock network of claim 8 further comprising:

at least one differential buffer connected to the dedicated input-clock pin;

at least one phase-lock loop connected to the differential buffer;

a phase-lock loop output multiplexing block connected to the phase-lock loop; and

at least one multiplexer having:

a first input connected directly to the dedicated input-clock pin,

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a second input connected directly to the output of the differential buffer,

a third input connected to the output of the phase-lock loop output multiplexing block, and

a fourth input connected to a sneak path from the at least one logic resource.

10.   A clock network for a programmable logic device (PLD), wherein the PLD includes a first set of logic resources and at least a second set of logic resources, the clock network comprising:

a first set of clock lines configured to distribute clock signals to the first set of logic resources separately from the second set of logic resources; and

a second set of clock lines configured to distribute clock signals to the second set of logic resources separately from the first set of logic resources.

11.   The clock network of claim 10 further comprising:

a third set of clock lines configured to distribute clock signals to both the first and second sets of logic resources.

12.   The clock network of claim 11, wherein the third set of clock lines receives an input-clock signal from a sneak path of at least one logic resource.

13.   The clock network of claim 12, wherein the third set of clock lines receives an input-clock signal from a dedicated input-clock pin.

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14.   The clock network of claim 13, wherein the third set of clock lines is connected to at least one multiplexer having at least one input connected to the dedicated input-clock pin and at least one input connected to the sneak path of a logic resource.

15.   The clock network of claim 11 further comprising:

a first central line that connects to the first and third sets of lines and to each logic resource in the first set of logic resources; and

a second central line that connects to the second and third sets of lines and to each logic resource in the second set of logic resources.

16.   The clock network of claim 15, where the first and second central lines receive input-clock signals from input pins of the integrated circuit that are not dedicated as input-clock pins.

17.   A method for distributing clock signals within an integrated circuit using a clock network comprising:

distributing clock signals to a first section of the integrated circuit using a first set of lines of the clock network; and

distributing clock signals to a second section of the integrated circuit separately from the first section using a second set of lines of the clock network.

18.   The method of claim 17 further comprising:

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distributing clock signals to both the first and second sections of the integrated

circuit through a third set of lines of the clock network.

19.   The method of claim 17 further comprising:

receiving input-clock signals from a logic resource on the integrated circuit.

20.   The method of claim 17 further comprising:

receiving input-clock signals from input pins on the integrated circuit that are not

dedicated as input-clock pins.